Performance Enhancement for 14nm High Volume Manufacturing Microprocessor and System on a Chip Processes

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Abstract

We describe here performance enhancement to Intel's 14nm high-performance logic technology interconnects and back end stack and introduce the SOC technology family of interconnects. Enhancement includes improved RC performance and intrinsic capacitance for back end metal layers over a range of process versions and metal stacks offered for optimal cost and density targeted for various applications.

Introduction

Intel offers a wide range of BE interconnect stacks which allow for a wide range of pitches and performance options. As the amount of products supported grows so does the need for flexibility when designing the interconnects with respect to not only density and performance but also cost and added features. As these BE options are developed, so too is the original logic technology enhanced. As the yields have matured on Intel's logic technology [1,2] the BE has been optimized to provide better performance. This enhancement is produced without any inherent loss of reliability or yield.

BE stack options which provide an idea of the range of possible options are presented in Table 1. Options can vary as little as changing the pitch at a single layer (SOC to V1) to adding three more layers (SOC to V3) or something in between (V2). The SOC high density interconnect stack is shown in Fig.1 next to the 14nm high performance logic interconnect stack. In addition to the logic stack [2] the table shows four SOC options which cover a wide range of cost, performance, and interconnect density. The table also indicates the dielectrics employed at each layer. In general Layers running pitch < 80nm employ Intel's Self Aligned Double Patterning process (SADP) [2] with self aligned vias. The inherent alignment advantages of the SADP integration scheme enable employing 6 layers of dense pitch interconnects in the SOC interconnect stack, 4 of

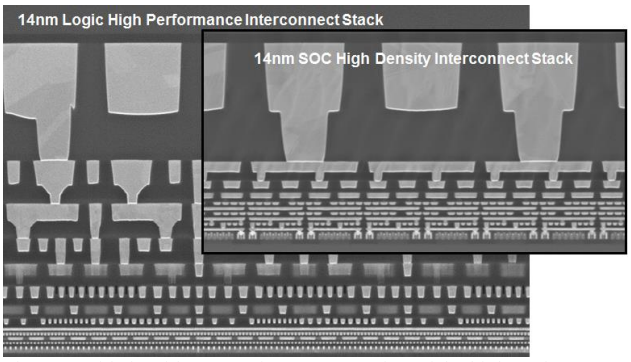

Figure 1. Side by side comparison cross section of the high performance logic interconnect stack vs. the high density SOC stack (inset).

Table 1: Back End Stack Interconnects for Intel's Logic (CPU) stack in addition to four versions of SOC interconnects.

Layers	CPU	SOC	*V1*	*V2*	V3
M0 / VCN	56nm	56nm	56nm	56nm	56nm
M1 / V0	70nm	70nm	70nm	70nm	70nm
M2 /V1	52nm	52nm	52nm	52nm	52nm
M3 / V2	56nm	52nm	52nm	52nm	52nm
M4 / V3	80nm	52nm	52nm	80nm	52nm
M5/ V4	100nm	52nm	52nm	80nm	80nm
M6 / V5	160nm	80nm	80nm	80nm	80nm
M7 / V6	160nm	112nm	112nm	112nm	112nm
M8 / V7	160nm	252nm	160nm	160nm	160nm
M9 / V8	252nm	1080nm	1080nm	1080nm	160nm
M10 / V9	252nm	-	-	4000nm	252nm
M11 / V10	1080nm	-	-	-	252nm
M12/V11	-	-	-	-	1080nm
MIM/Vx	3-Plate	2-plate	2-plate	2-plate	2-plate
TM1	14um	11um	11um	11um	11um
Bump	130um	130um	78um & 130um	130um	55um & 130um

Layers	CPU	SOC	*V1*	*V2*	V3
M0 / VCN	LK CDO	LK CDO	LK CDO	LK CDO	LK CDO
M1 / V0	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M2 /V1	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M3 / V2	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M4 / V3	Air Gap	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M5/ V4	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M6 / V5	Air Gap	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M7 / V6	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M8 / V7	ULK CDO	ULK CDO	ULK CDO	ULK CDO	ULK CDO
M9 / V8	LK CDO	Oxide	Oxide	Oxide	ULK CDO
M10 / V9	LK CDO	- -	- -	Oxide	LK CDO
M11 / V10	Oxide	- -	- -	- -	LK CDO
M12/V11	- -	- -	- -	- -	Oxide
MIM	3 Plates	2 Plates	2 Plates	2 Plates	2 Plates
TV0	Nitride	Nitride	Nitride	Nitride	Nitride
TM1	Polymer	Polymer	Polymer	Polymer	Polymer
Bump	Copper	Copper	Copper	Copper	Copper

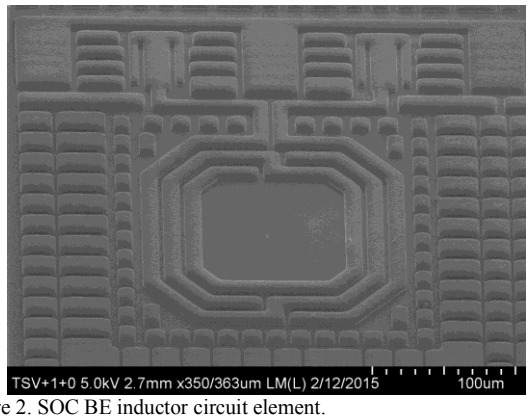

Figure 2. SOC BE inductor circuit element.

which are 52nm pitch.

Pitches 80nm up to 160nm run a trench first self aligned via process while those with pitches >160nm are a via first process. All are dual damascene except TM1 which is a plate up process.

Where higher decap capacitance is not required Intel offers a reduced cost Dual plate MIM capacitor similar to the one first introduced in Intel's 22nm process [3]. For RF applications the SOC process also offers the option of using high resistance Silicon and additional circuit elements such as the inductor element is shown in Fig.2. The inductor utilizes 45 degree Thick Metal 1(TM1) lines to give a 20% inductance improvement over the same inductor drawn with 90 degree turns.

Pitch Doubling Enhancement

In 14nm a wide range of pitch and layer combinations are offered. The lower layers are similar and this allows reuse of key IP blocks and optimized cell layouts. As we move up in the interconnect stack product designer can use the CPU stack which focus on performance and includes the use of an air gap layer at MT4 and MT6 for a 17% Capacitance improvement [2]. Or if the focus is on density then the SOC stack offers dense interconnects through MT5. To save cost an overall reduced number of metal layers is offered when long high performance routing is not required. And for when RF performance is required high resistance substrates and wide pitches can be employed. Customization is offered within the SOC stacks as well to allow products to optimize a given layer's R vs C trade-off targets by up to 30%. This is managed by engineering the aspect ratio of any given layer.

In 14nm there has been a continuous improvement for RC enhancement. As seen in Fig.3a the enhanced process demonstrates a 9% decrease in the capacitance as compared to the logic process at the time of lead product launch. This was not accomplished thru a change in the

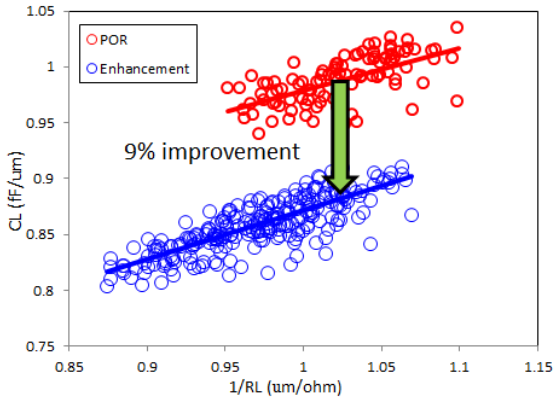

Figure 3a. Capacitance vs inverse resistance normalized for Intel's SOC M2 pitch division layer showing 9% benefit on performance enhancement process.

deposited dielectric film. Instead the improvements come from process improvements: taller Vias (reduced layer to layer capacitance), less process damage to ILD (improved end of line dielectric k), Copper polish improvements to prevent dishing (impacts R without degrading Cap) and a change in both barrier film deposition and the thickness to improve volume of Cu within the interconnect.

These changes were made with no loss in reliability performance. By changing the film disposition from bi-layer to single layer a significant benefit was seen EM performance. This enabled barrier scaling for significant resistance reduction while still exceeding the product reliability requirements. This is shown in Fig 3b, which shows the Mean time to fail for the bi-layer film and the single layer deposition in four thickness 1X, 0.85X, 0.77X and 0.70X with the 0.77X film being used in production. This change not only reduced interconnect RC but also resulted in a reduction in Via resistance by an average of 30%. This improvement in trench and lower via resistance provides a significant performance enhancement.

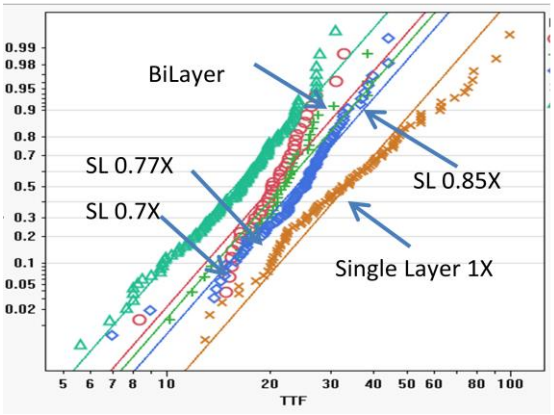

Figure 3b. Time To Fail EM plot for full range of performance enhancement skews on the barrier process. The single film 0.7x barrier matches the EM performance of the thicker Bilayer barrier.

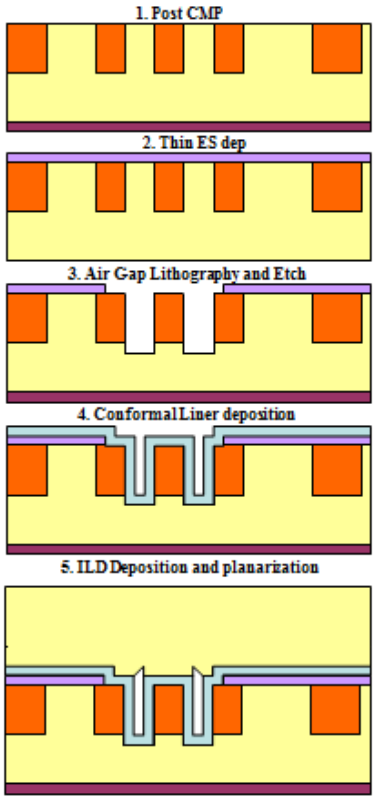

Figure 4. air gap integration process sequence. Enhanced performance can be obtained thru extending the step 3 etch.

Air Gap Process Enhancement

Performance enhancement for Intel's air gap process has been developed. The process flow schematic is shown in Fig. 4. The process flow consists of a single masking layer to control placement of the air gap and then a subsequent etch which is selective to the Metal interconnect. The etch labeled step 3 in the figure provides the ability to reduce the line to line capacitance within the air gap layer.

Depths reaching the surface of the etch stop layer on top of the layer below have been tested, however, the practical depth is limited by the conformality of the air gap liner shown in step 4 in Fig.4. As the conformality of the liner becomes stressed the liner develops pinholes which induce subsequent layer patterning problems. Reasonable depth increases, however, do yield improved capacitance. Fig. 5 shows the effect of skewing the air gap deeper. Capacitance decreases rather linearly for depth perturbations around the depth of the metal. Every air gap depth increases of 10nm demonstrates a 4% reduction in total capacitance with no impact to interconnect resistance.

The air gap interconnect Reliability is enhanced thru engineering of the metal composition. Fine tuning of the metal process including optimization of the metal barrier and subsequent thermal budget prior to liner deposition were also employed to enhance the air gap interconnect RC performance. Resulting interconnects continue to meet all electromigration standards.

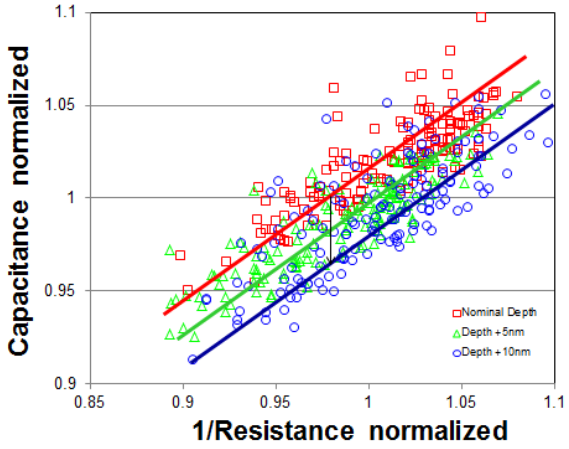

Figure 5. Capacitance vs inverse resistance normalized for Intel's 80nm pitch air gap layer as a function of air gap depth

Summary

Intel continues to enhance performance of the interconnect stack even as it offers additional stack options for its SOC line of products. New features have been added and this enhancement has not come at the cost of reliability or yield.

The customizable interconnect stacks allow greater versatility for products and allow for the optimization of features, cost, performance and density. Both the logic interconnect stack as well as the SOC based back end are currently in high volume in multiple worldwide fabrication facilities. 14nm high volume yields have continued to mature and now approach historical end of technology goals.

Acknowledgements

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